M16C/80, M32C/84 Group

Differences between M16C/80 and M32C/84

1. Abstract

The following document describes differences between M16C/80 and M32C/84.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/80, M32C/84 Group

3. Contents

3.1 Function Differences

Table 3.1.1 and Table 3.1.3 show the Function Differences.

Table 3.1.1 Function Differences (1) (Note1)

Item	M16C/80	M32C/84
Basic Instructions	106 instructions	108 instructions (Add SHANC, SHLNC instructions)
Shortest Instruction Execution Time	50ns(f(XIN)=20MHz)	31.3ns(f(BCLK)=32MHz)
I/O power supply	Single (VCC)	Double (VCC1, VCC2)
Supply Voltage	4.2V to 5.5V(f(XIN)=20MHz) 2.7V to 5.5V(f(XIN)=10MHz)	VCC1=4.2V to 5.5V, VCC2=3.0V to VCC1 (f(BCLK)=32MHz) VCC1=3.0V to 5.5V, VCC2=3.0V to VCC1 (f(BCLK)=24MHz)
Clock Generating Circuit	XIN, XCIN	XIN, XCIN, PLL, On-chip oscillator
Main clock drive capability select function	Have	None
System Clock Protect Function	None	Have
Peripheral Function clock	f1, f8, f32, fC32	f1, f8, f2n, fC32 (n=0 ot 15. No division when n=0)
Oscillation Stop Detect Function	None	Have
Voltage Detection Circuit	None	Have
Power Consumption	45mA(5V, f(XIN)=20MHz) 14mA(3V, f(XIN)=10MHz) 1.5μA (3V, f(XCIN)=32kHz, drive capacity Low)	28mA (VCC1= VCC2=5V, f(BCLK)=32MHz) 22mA (VCC1= VCC2=3.3V, f(BCLK)=24MHz) 10μA (VCC1= VCC2=3.3V, f(XCIN)=32kHz, in wait mode)
Access to SFR	1 wait fixed	Variable (1 to 2 waits)
Bus wait	No wait to 3 waits (Select WCR register)	1 wait to 8 waits (Select EWCR0 to EWCR3 register)
Recovery Cycle	Not available	Available
Protect	Can be set for PM0, PM1, CM0, CM1, MCD, PD9, PS3 register	Can be set for PM0, PM1, CM0, CM1, MCD, PD9, PS3, CM2, PLC0, PLC1, PM2, INVC0, INVC1, VCR2, D4INT register
Address Match Interrupt	Set in four addresses	Set in eight addresses

Note 1: About the details and the characteristics, refer to hardware manual.

Table 3.1.2 Function Differences (2) (Note1)

Item	M16C/80	M32C/84
DMA Request Factors	Falling edge or both edges of input signals to the INT0 to INT3 pin Timer A0 to timer A4 interrupt requests Timer B0 to timer B5 interrupt requests UART0 to UART4 transmit and receive interrupt requests A/D conversion interrupt request Software trigger	The next interrupt is added to M16C/80. Intelligent I/O interrupt request CAN interrupt request
DMACII Function	None	Have
Timer A, Timer B Count Source	Selectable: f1, f8, f32, fC32	Selectable: f1, f8, f2n, fC32 (n=0 to 15,.No division when n=0)
Three-Phase Motor Control Timer Dead Time	Have	Selectable
Three-Phase Motor Control Timer Dead Time Trigger	Fixed	Selectable
Three-Phase Motor Control Timer Count Source	Selectable: f1, f8, f32, fC32	Selectable: f1, f8, f2n, fC32 (n=0 to 15. No division when n=0)
Serial I/O	(Clock synchronous serial I/O, Clock asynchronous serial I/O) × 2 (Clock synchronous serial I/O, Clock asynchronous serial I/O , I2C bus™ (Note 2), IEBus™(Note 3), SIM interface) × 3	(Clock synchronous serial I/O, Clock asynchronous serial I/O, I2C bus™ (Note 2), IEBus™(Note 3), GCI bus, SIM interface) × 5
Serial I/O CTS/RTS Separate Function	Can be used in UART0	None
Serial I/O Transfer Clock Output from Multiple Pins	Can be used in UART1	None
Serial I/O TxD, RxD I/O Polarity Switching Function	Can be used in UART2 to UART4	Can be used in UART0 to UART4
Serial I/O Sleep Function	Can be used in UART0, UART1	None
Serial I/O Count Source	Selectable: f1, f8, f32	f1, f8, f2n(n=0 to 15. No division when n=0)
Serial I/O Overrun error occur timing	This error occurs when the next data is ready before contents of UiRB register (i=0 to 4) are read out	This error occurs if the serial I/O started receiving the next data before reading the UiRB register (i=0 to 4) and received the 7th bit of the next data (Clock synchronous serial I/O). This error occurs if the serial I/O started receiving the next data before reading the UiRB register and received the bit one before the last stop bit of the next data (Clock asynchronous serial I/O).
Serial I/O UART Mode RTS Timing	Assert low when reception is completed	Assert low when receive buffer is read
Serial I/O I2C Mode	Start condition, stop condition: Not auto-generation	Start condition, stop condition: Auto-generation
Serial I/O I2C mode SDA delay	SDA digital delay count source: 1/f(XIN)	SDA digital delay count source: BRG
CAN Module	None	1 channel
Intelligent I/O	None	1 group
A/D Converter	1 circuit, 10 channels	1 circuits, 34 channels (26 channel: 100-pin version)

Note 1: About the details and the characteristics, refer to hardware manual.
Note 2: I2C bus is a trademark of Koninklijke Philips Electronics N. V.
Note 3: IEBus is a trademark of NEC Electronics Corporation.

Table 3.1.3 Function Differences (3) (Note1)

Item	M16C/80	M32C/84
A/D Converter Maximum Operating Frequency	10MHz	16MHz (VCC1= VCC2=5.0V)
A/D Converter Operating Clock	Selectable: fAD, fAD/2, fAD/4	Selectable: fAD, fAD/2, fAD/3, fAD/4, , fAD/6, fAD/8
A/D Converter Mode	One-shot mode, repeat mode, single sweep mode, repeat sweep mode 0, repeat sweep mode 1	The next mode is added to M16C/80. Multi-port single sweep mode, multi-port repeat sweep mode 0
A/D Converter DMAC Operating Mode	None	Have
DRAMC	Have	None
Flash Memory Program	Per page	Per word, per byte (Note 2)
Flash Memory Rewrite Mode	CPU rewrite mode (EW mode 0 corresponding)	EW mode 0, EW mode 1
Flash Memory Standard Serial I/O Mode	Clock synchronous serial I/O, Clock asynchronous serial I/O	Clock synchronous serial I/O, Clock asynchronous serial I/O, CAN
Flash Memory Boot ROM	8K bytes	4K bytes
Flash Memory Block A	None	Have (4K bytes)
Flash Memory Block	Block 0: 16K bytes Block 1: 8K bytes Block 2: 8K bytes Block 3: 32K bytes Block 4 or more: 64K bytes	Block 0: 4K bytes Block 1: 4K bytes Block 2: 8K bytes Block 3: 8K bytes Block 4: 8K bytes Block 5: 32K bytes Block 6 or more: 64K bytes
Flash Memory Software Command Program	“41h” is written in the first bus cycle. Data to the write address in the second bus cycle to 129th bus cycle.	“xx40h” is written in the first bus cycle. Data to the write address in the second bus cycle.
Flash Memory Software Command Read Lock Bit Status	“71h” is written in the first bus cycle. Read lock bit status in the second bus cycle.	“xx71h” is written in the first bus cycle. “xxD0h” is written in the second bus cycle. Read the FMR16 bit in the FMR1 register.

Note 1: About the details and the characteristics, refer to hardware manual.

Note 2: Programming per byte is available in parallel I/O mode only.

3.2 Pin function Differences

Table 3.2.1 and Table 3.2.2 show the Pin Function Differences.

Table 3.2.1 Pin Function Differences (1/2)

M16C/80	M32C/84	Remarks
P14$_3$	P14$_3$/INPC17/OUTC17	Add INPC17/OUTC17
P14$_2$	P14$_2$/INPC16/OUTC16	Add INPC16/OUTC16
P14$_1$	P14$_1$/INPC15/OUTC15	Add INPC15/OUTC15
P14$_0$	P14$_0$/INPC14/OUTC14	Add INPC14/OUTC14
P8$_3$/$\overline{INT1}$	P8$_3$/$\overline{INT1}$/CAN0$_{IN}$	Add CAN0$_{IN}$
P8$_2$/$\overline{INT0}$	P8$_2$/$\overline{INT0}$/CAN0$_{OUT}$	Add CAN0$_{OUT}$
P8$_1$/TA4$_{IN}$/$\overline{U}$	P8$_1$/TA4$_{IN}$/$\overline{U}$/INPC15/OUTC15	Add INPC15/OUTC15
P8$_0$/TA4$_{OUT}$/U	P8$_0$/TA4$_{OUT}$/U/ISRxD0	Add ISRxD0
P7$_7$/TA3$_{IN}$	P7$_7$/TA3$_{IN}$/INPC14/OUTC14/ISCLK0/CAN0$_{IN}$	Add INPC14/OUTC14/ISCLK0/CAN0$_{IN}$
P7$_6$/TA3$_{OUT}$	P7$_6$/TA3$_{OUT}$/INPC13/OUTC13/ISTxD0/CAN0$_{OUT}$	Add INPC13/OUTC13/ISTxD0/CAN0$_{OUT}$
P7$_5$/TA2$_{IN}$/$\overline{W}$	P7$_5$/TA2$_{IN}$/$\overline{W}$/INPC12/OUTC12/ISRxD1/BE1$_{IN}$	Add INPC12/OUTC12/ISRxD1/BE1$_{IN}$
P7$_4$/TA2$_{OUT}$/W	P7$_4$/TA2$_{OUT}$/W/INPC11/OUTC11/ISCLK1	Add INPC11/OUTC11/ISCLK1
P7$_3$/$\overline{V}$/$\overline{CTS2}$/$\overline{RTS2}$/TA1$_{IN}$	P7$_3$/$\overline{V}$/$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$/TA1$_{IN}$/INPC10/OUTC10/ISTxD1/BE1$_{OUT}$	Add INPC10/OUTC10/ISTxD1/$\overline{SS2}$ /BE1$_{OUT}$
P7$_1$/RxD2/SCL2/TA0$_{IN}$/TB5$_{IN}$	P7$_1$/RxD2/SCL2/TA0$_{IN}$/TB5$_{IN}$/STxD2/INPC17/OUTC17	Add STxD2/INPC17/OUTPC17
P7$_0$/TxD2/SDA2/TA0$_{OUT}$	P7$_0$/TxD2/SDA2/TA0$_{OUT}$/INPC16/SRxD2/OUTC16	Add SRxD2/INPC16/OUTC16
P6$_7$/TxD1	P6$_7$/TxD1/SDA1/SRxD1	Add SDA1/SRxD1
P6$_6$/RxD1	P6$_6$/RxD1/SCL1/STxD1	Add SCL1/STxD1
P6$_4$/$\overline{CTS1}$/$\overline{RTS1}$/$\overline{CTS0}$/CLKS1	P6$_4$/$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$	Add $\overline{SS1}$ Delete $\overline{CTS0}$/CLKS1
P6$_3$/TxD0	P6$_3$/TxD0/SDA0/SRxD0	Add SDA0/SRxD0
P6$_2$/RxD0	P6$_2$/RxD0/SCL0/STxD0	Add SCL0/STxD0
P6$_0$/$\overline{CTS0}$/$\overline{RTS0}$	P6$_0$/$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$	Add $\overline{SS0}$
P5$_6$/ALE/$\overline{RAS}$	P5$_6$/ALE	Delete $\overline{RAS}$
P5$_2$/$\overline{RD}$/$\overline{DW}$	P5$_2$/$\overline{RD}$	Delete $\overline{DW}$
P5$_1$/$\overline{WRH}$/$\overline{BHE}$/$\overline{CASH}$	P5$_1$/$\overline{WRH}$/$\overline{BHE}$	Delete $\overline{CASH}$
P5$_0$/$\overline{WRL}$/$\overline{WR}$/$\overline{CASL}$	P5$_0$/$\overline{WRL}$/$\overline{WR}$	Delete $\overline{CASL}$
P4$_4$/$\overline{CS3}$/A$_{20}$(MA12)	P4$_4$/$\overline{CS3}$/A$_{20}$	Delete MA12
P4$_3$/A$_{19}$(MA11)	P4$_3$/A$_{19}$	Delete MA11
P4$_2$/A$_{18}$(MA10)	P4$_2$/A$_{18}$	Delete MA10
P4$_1$/A$_{17}$(MA9)	P4$_1$/A$_{17}$	Delete MA9
P4$_0$/A$_{16}$(MA8)	P4$_0$/A$_{16}$	Delete MA8
P3$_7$/A$_{15}$(MA7)(/D$_{15}$)	P3$_7$/A$_{15}$(/D$_{15}$)	Delete MA7
P3$_6$/A$_{14}$(MA6)(/D$_{14}$)	P3$_6$/A$_{14}$(/D$_{14}$)	Delete MA6
P3$_5$/A$_{13}$(MA5)(/D$_{13}$)	P3$_5$/A$_{13}$(/D$_{13}$)	Delete MA5
P3$_4$/A$_{12}$(MA4)(/D$_{12}$)	P3$_4$/A$_{12}$(/D$_{12}$)	Delete MA4
P3$_3$/A$_{11}$(MA3)(/D$_{11}$)	P3$_3$/A$_{11}$(/D$_{11}$)	Delete MA3
P3$_2$/A$_{10}$(MA2)(/D$_{10}$)	P3$_2$/A$_{10}$(/D$_{10}$)	Delete MA2
P3$_1$/A$_9$(MA1)(/D$_9$)	P3$_1$/A$_9$(/D$_9$)	Delete MA1
P3$_0$/A$_8$(MA0)(/D$_8$)	P3$_0$/A$_8$(/D$_8$)	Delete MA0

Table 3.2.2 Pin Function Differences (2/2)

M16C/80	M32C/84	Remarks
P27/A7(/D7)	P27/A7(/D7)/AN27	Add AN27
P26/A6(/D6)	P26/A6(/D6)/AN26	Add AN26
P25/A5(/D5)	P25/A5(/D5)/AN25	Add AN25
P24/A4(/D4)	P24/A4(/D4)/AN24	Add AN24
P23/A3(/D3)	P23/A3(/D3)/AN23	Add AN23
P22/A2(/D2)	P22/A2(/D2)/AN22	Add AN22
P21/A1(/D1)	P21/A1(/D1)/AN21	Add AN21
P20/A0(/D0)	P20/A0(/D0)/AN20	Add AN20
P07/D7	P07/AN07/D7	Add AN07
P06/D6	P06/AN06/D6	Add AN06
P05/D5	P05/AN05/D5	Add AN05
P04/D4	P04/AN04/D4	Add AN04
P113	P113/OUTC13/INPC13	Add OUTC13/INPC13
P112	P112/OUTC12/INPC12/ISRxD1/BE1IN	Add OUTC12/INPC12/ISRxD1/BE1IN
P111	P111/OUTC11/INPC11/ISCLK1	Add OUTC11/INPC11/ISCLK1
P110	P110/OUTC10/INPC10/ISTxD1/BE1OUT	Add OUTC10/INPC10/ISTxD1/BE1OUT
P03/D3	P03/AN03/D3	Add AN03
P02/D2	P02/AN02/D2	Add AN02
P01/D1	P01/AN01/D1	Add AN01
P00/D0	P00/AN00/D0	Add AN00
P157	P157/AN157	Add AN157
P156	P156/AN156	Add AN156
P155	P155/AN155	Add AN155
P154	P154/AN154	Add AN154
P153	P153/AN153	Add AN153
P152	P152/AN152/ISRxD0	Add AN152/ISRxD0
P151	P151/AN151/ISCLK0	Add AN151/ISCLK0
P150	P150/AN150/ISTxD0	Add AN150/ISTxD0

3.3 SFR Differences

Table 3.3.1 and Table 3.3.3 show the SFR Differences.

Table 3.3.1 SFR Differences (1/3)

M16C/80	M32C/84	Remarks
PM1	PM1	Add bit 3. Change set value of reserved bit.
CM0	CM0	Change function
CM1	CM1	Add bit 7. Delete bit 5. Change function.
WCR	-	
AIER	AIER	Add bits 4 to 7
PRCR	PRCR	Add bit 3. Change function.
-	CM2	
WDC	WDC	Add bit 5
-	PM2	
-	VCR2	
-	VCR1	
-	PLC0	
-	PLC1	
-	RMAD4	
-	RMAD5	
-	D4INT	
-	RMAD6	
-	RMAD7	
DRAMCONT	-	
REFCNT	-	
-	EWCR0	
-	EWCR1	
-	EWCR2	
-	EWCR3	
BCN3IC	BCN0IC/BCN3IC	Shard with BCN0IC register
ADIC	AD0IC	Change register name
BCN4IC	BCN1IC/BCN4IC	Shard with BCN1IC register
RLVL	RLVL	Add bit 5
-	Intelligent I/O, CAN related interrupt control register	
-	Intelligent I/O interrupt request register	
-	Intelligent I/O interrupt enable register	
-	Intelligent I/O related register	
-	IPS	
-	IPSA	
-	CAN related register	
-	U4SMR4	
U4SMR2	U4SMR2	Change function
U4SMR	U4SMR	Add bit 7
U4C0	U4C0	Change function
U4C1	U4C1	Change function

Table 3.3.2 SFR Differences (2/3)

M16C/80	M32C/84	Remarks
INVC1	INVC1	Add bits 5, 6
IFSR	IFSR	Add bits 6, 7
-	U3SMR4	
U3SMR2	U3SMR2	Change function
U3SMR	U3SMR	Add bit 7
U3C1	U3C1	Change function
-	U2SMR4	
U2SMR3	U2SMR3	Add bits 0 to 4
U2SMR2	U2SMR2	Change function
U2SMR	U2SMR	Add bit 7
U2C1	U2C1	Change function
-	TB2SC	
-	TCSPR	
-	U0SMR4	
-	U0SMR3	
-	U0SMR2	
-	U0SMR1	
-	U0SMR	
U0MR	U0MR	Address change from 0360h to 0368h. Change function.
U0BRG	U0BRG	Address change from 0361h to 0369h.
U0TB	U0TB	Address change from 0363h-0362h to 036Bh-036Ah.
U0C0	U0C0	Address change from 0364h to 036Ch
U0C1	U0C1	Address change from 0365h to 036Dh. Add bits 4 to 7.
U0RB	U0RB	Address change from 0367h-0366h to 036Fh-036Eh
-	U1SMR4	
-	U1SMR3	
-	U1SMR2	
-	U1SMR	
U1MR	U1MR	Address change from 0368h to 02E8h. Change function.
U1BRG	U1BRG	Address change from 0369h to 02E9h.
U1TB	U1TB	Address change from 036Bh-036Ah to 02Ebh-02Eah
U1C0	U1C0	Address change from 036Ch to 02Ech
U1C1	U1C1	Address change from 036Dh to 02Edh. Add bits 4 to 7.
U1RB	U1RB	Address change from 036Fh-036Eh to 02Efh-02EEh
UCON	-	
FMR1	FMR1	Address change from 0376h to 0055h. Add bits 1, 6. Delete bit 3.
FMR0	FMR0	Address change from 0377h to 0057h. Add bits 6, 7. Change function
DM0SL	DM0SL	Change function
DM1SL	DM1SL	Change function
DM2SL	DM2SL	Change function
DM3SL	DM3SL	Change function
AD0	AD00	Change register name
AD1	AD01	Change register name
AD2	AD02	Change register name
AD3	AD03	Change register name
AD4	AD04	Change register name

Table 3.3.3 SFR Differences (3/3)

M16C/80	M32C/84	Remarks
AD5	AD05	Change register name
AD6	AD06	Change register name
AD7	AD07	Change register name
-	AD0CON4	
ADCON2	AD0CON2	Change register name. Add bits 1, 2, 5.
-	AD0CON3	
ADCON0	AD0CON0	Change register name. Change function.
ADCON1	AD0CON1	Change register name. Change function.
-	PS8	
-	PS9	
-	PSD1	
-	PSC2	
-	PSC3	
PSC	PSC	Add bits 1 to 4, 6. Change function.
PS0	PS0	Add bits 2, 6. Change function.
PS1	PS1	Add bit 7. Change function.
PSL0	PSL0	Add bits 2, 6. Change function.
PSL1	PSL1	Add bits 1, 5 to 7. Change function.
PS2	PS2	Add bit 2. Change function.
PS3	PS3	Change function
PSL2	PSL2	Add bits 1, 2.
PSL3	PSL3	Add bit 2
-	PS5	

3.4 Interrupt Vector Differences

Table 3.4.1 shows the Fixed Vector Table Differences. Table 3.4.2 shows the Relocatable Vector Table Differences.

Table 3.4.1 Fixed Vector Table Differences

M16C/80 Interrupt Factor	M32C/84 Interrupt Factor	Remarks
Watchdog Timer	Watchdog Timer Oscillation Stop Detection Low Voltage Detection	Add oscillation Stop Detection, Low Voltage Detection

Table 3.4.2 Relocatable Vector Table Differences

M16C/80 Interrupt Factor	M32C/84 Interrupt Factor	Software Interrupt Number
UART0 transmission	UART0 transmission, NACK	17
UART0 reception	UART0 reception, ACK	18
UART1 transmission	UART1 transmission, NACK	19
UART1 reception	UART1 reception, ACK	20
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect (UART2)	Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART2)	39
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART3)	Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART3 or UART0)	40
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART4)	Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART4 or UART1)	41
-	Intelligent I/O Interrupt 0	44
-	Intelligent I/O Interrupt 1	45
-	Intelligent I/O Interrupt 2	46
-	Intelligent I/O Interrupt 3	47
-	Intelligent I/O Interrupt 4	48
-	Intelligent I/O Interrupt 8	52
-	Intelligent I/O Interrupt 9, CAN0	53
-	Intelligent I/O Interrupt 10, CAN1	54
-	CAN2	57

3.5 I/O Port Power Supply Voltage Differences

Power supplies which relate to the external bus pins are separated as VCC2, thus they can be interfaced using the different voltage as VCC1. Table 3.5.1 shows I/O Port Power Supply Voltage Differences

Table 3.5.1 I/O Port Power Supply Voltage Differences

	M16C/80 I/O Port Power Supply Voltage	M32C/84 I/O Port Power Supply Voltage
P0 to P5, P11 to P13	V_{CC}	V_{CC2}
P6 to P10, P14 to P15	V_{CC}	V_{CC1}

3.6 Support Tool Differences

Table 3.6.1 shows the support tool differences.

Table 3.6.1 Support Tool Differences

Tool information	M16C/80 Tool Product	M32C/84 Tool Product
C Compiler	M3T-NC308WA	M3T-NC308WA
Real-time OS	M3T-MR308	M3T-MR308
Simulator Debugger	M3T-PD308SIM	M3T-PD308SIM
Emulator Debugger	M3T-PD308	M3T-PD308F
Emulator	PC4701U	PC7501
Emulation Pod, Emulation Probe	M30803T-RPD-E	M30850T-EPB
Compact Emulator	M30800T-CPE	M30850T2-CPE

4. Reference

Renesas Technology Corporation Home Page

http://www.renesas.com/

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Hardware Manual

M32C/84 Group Hardware Manual
(Use the latest version on the home page: http://www.renesas.com)

User's Manual

M16C/80 Group User's Manual
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